

PATENT ABSTRACTS OF JAPAN

(11)Publication number : 05-144971

(43)Date of publication of application : 11.06.1993

(51)Int.Cl.

H01L 23/12
H01L 23/40

(21)Application number : 03-329586

(71)Applicant : NEC CORP

(22)Date of filing : 18.11.1991

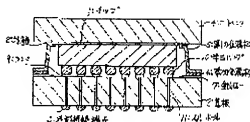
(72)Inventor : MIYAZAKI YUICHI

(54) STRUCTURE OF CHIP CARRIER

(57)Abstract:

PURPOSE: To reduce a voltage drop in a circuit board to be used for a chip carrier and to decrease a signal propagation delay and noise by employing a straight line wiring from a chip terminal to external connection terminal thereby minimizing the length of inner wiring of a chip carrier board.

CONSTITUTION: A chip carrier connects a chip 1 to a board 2 via a solder bump 10 and a land 9, and further airtightly seal the chip 1 via the board 2, a first metal frame 5, a second metal frame 6 and a heat sink 4. The board 2 has a straight through hole 11, which connects the land 9 to an external connection terminal 3 for connecting the chip 1 to the outside of chip carrier 2 via a straight conductor wiring, thereby mostly shortening the wiring length. Thus, a signal wiring length in the board 2 becomes short to reduce a signal delay and noise. The wiring length of a power source is also shortened, and a voltage drop is reduced.



LEGAL STATUS

[Date of request for examination] 27.10.1995

[Date of sending the examiner's decision of rejection] 30.09.1997

[Kind of final disposal of application other than the examiner's decision of rejection or application converted registration]

[Date of final disposal for application]

[Patent number]

[Date of registration]

[Number of appeal against examiner's decision of rejection]

[Date of requesting appeal against examiner's decision of rejection]

[Date of extinction of right]